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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,644	09/05/2006	Kenichi Horiguchi	1163-0582PUS1	1802
2292 7590 09/30/2008 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				
EXAMINER NGUYEN, PATRICIA T				
ART UNIT		PAPER NUMBER		
2817				
NOTIFICATION DATE		DELIVERY MODE		
09/30/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary

Application No.

10/591,644

Applicant(s)

HORIGUCHI ET AL.

Examiner

PATRICIA T. NGUYEN

Art Unit

2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3-11 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 3-8, 10 and 11 is/are rejected.
- 7) ☒ Claim(s) 9 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF/ICE)
Paper No(s)/Mail Date 4/10/08, 8/13/08, 9/12/08
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3-7, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hellberg, WO 01/95481.

Figs. 14 and 15 of Hellberg disclose a circuit comprising: A high efficiency amplifier including input signal dividing means (10) for splitting an input signal comprising: a first amplifier (PA1) for amplifying a first input signal fed from said input signal dividing means; a second amplifier (PA2) for amplifying, when power of a second input signal fed from said input signal dividing means is greater than specified power, the second input signal; and a combining circuit (couplers at outputs of PA1-PA5 having transmission lines of $\lambda/4$) for combining an output signal of said first amplifier and an output signal of said second amplifier, said high efficiency amplifier comprising before said first amplifier: amplifier; a level limiting circuit (L1) for limiting, when amplitude of the first input signal fed from said input signal dividing means is greater than a specified level, the amplitude of the first input signal to less than the specified level, and for supplying to said first amplifier.

Regarding claim 5, amplifier DR together with limiter L1 can be read as a level limiting circuit is a driver amplifier.

Regarding claims 6, 7, and 10, L1 and L2 can be read as waveform shaping circuit or first waveform shaping circuit and second waveform shaping circuit.

Claims 3, 4, 6-8, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hellberg, U.S. Publication # 2003/0137346 A1.

Figs. 16 and 17 of Hellberg disclose a circuit comprising: A high efficiency amplifier including input signal dividing means (input coupler at input of 18 and 38) for splitting an input signal (x) comprising: a first amplifier (10) for amplifying a first input signal fed from said input signal dividing means; a second amplifier (12) for amplifying, when power of a second input signal fed from said input signal dividing means is greater than specified power, the second input signal; and a combining circuit (couplers at outputs of 10, 12, 16 having transmission line Z_t of $\lambda/4$) for combining an output signal of said first amplifier and an output signal of said second amplifier, said high efficiency amplifier comprising before said first amplifier: amplifier; and a level limiting circuit (38) for limiting, when amplitude of the first input signal fed from said input signal dividing means is greater than a specified level, the amplitude of the first input signal to less than the specified level, and for supplying to said first amplifier.

Regarding claims 6, 7, and 10, non-linear functions 38 and 18 can be read as waveform shaping circuit or first waveform shaping circuit and second waveform shaping circuit.

Regarding claim 8, filters 42, 44 (similar to filter 40) can be read as a first distortion compensating circuit and a second distortion compensating circuit.

Claims 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Ditcham, U.S. patent # 2,085,011.

Fig. 1 of Ditcham discloses a circuit comprising: A high efficiency amplifier including input signal dividing means (input transformer at input of 3 and 5) for splitting an input signal comprising: a first amplifier (4) for amplifying a first input signal fed from said input signal dividing means; a second amplifier (3) for amplifying, when power of a second input signal fed from said input signal dividing means is greater than specified power, the second input signal; and a combining circuit (decoupling means 6 at outputs of 4 and 5) for combining an output signal of said first amplifier and an output signal of said second amplifier, said high efficiency amplifier comprising before said first amplifier: amplifier; and a level limiting circuit (limiter 5) for limiting, when amplitude of the first input signal fed from said input signal dividing means is greater than a specified level, the amplitude of the first input signal to less than the specified level, and for supplying to said first amplifier.

Allowable Subject Matter

Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICIA T. NGUYEN whose telephone number is (571)272-1768. The examiner can normally be reached on 6:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PTN
September 24, 2008
/Patricia T Nguyen/
Primary Examiner, Art Unit 2817